REMARKS

In response to the Office Action dated March 27, 2002, Applicants respectfully request reconsideration and withdrawal of the objections to the disclosure and claims, and the rejection of the claims.

The Examiner's thorough review of the Application is noted, with appreciation. In response to the objections set forth in the Office Action, the specification and claims have been reviewed and revised to incorporate the Examiner's suggestions. In addition, a separate Request for Approval of Drawing Changes accompanies this Amendment, and proposes that Figures 18 and 19 be revised to include the legend "Prior Art."

Claims 1-20 were rejected under 35 U.S.C. §103, as being unpatentable over the Orimo et al patent in view of the Tanenbaum publication. In essence, the rejection considers the Orimo patent to disclose all of the claimed subject matter, with the exception of using a shared memory among a plurality of processors. With respect to this feature, the Office Action states that such a feature would be obvious, in view of the teachings of the Tanenbaum publication.

Applicants respectfully submit that it would not be obvious to combine the teachings of the Tanenbaum publication with those of the Orimo patent to arrive at the presently claimed invention. Furthermore, it is respectfully submitted that the Orimo patent does not disclose a number of features of the claimed invention, in addition to the use of a shared memory.

The present invention is directed to a system in which a plurality of processes are performed on a given piece of data, in a prescribed order. In an exemplary embodiment of

the invention described in the application, the data for each pixel of an input image might have processes such as log conversion, MTF correction, gamma correction and binarization performed on it, in that order. In accordance with the invention, a plurality of processors are employed to execute the respective processes. To enable the processors to operate in an asynchronous manner, the pixel data is stored in a common memory that is shared among the processors. To ensure that the various processors execute their respective processes on a given piece of data in the prescribed order, state information is also stored in the memory in association with the pixel data.

In contrast to the present invention, the Orimo patent is not concerned with a system in which multiple different processes are executed on data in a prescribed order. Rather, the patent discloses a multiple-execution method and system for multiple-version programs. As defined in the patent, multiple-version programs "means a plurality of programs for performing the same function but having different program structures." (column 1, lines 18-20) In the example illustrated in the patent, one simulation program for an event may have low calculation precision, and another simulation program for the same event may have high calculation precision. There is no prescribed order in which the different versions of the program are executed. In fact, they can be executed in parallel.

Referring to Figure 8, the first processor 11 executes an application program 51, and transmits the results of that execution as a message 510 over a network 1. Second and third processors 12 and 13 execute different versions 52a and 52b of an application program that perform the same simulation on the result from the application program 51. In response to receipt of the message 510, each of the processors 12 and 13 executes its

respective version of the application program, and transmits the execution results as messages 520a and 520b, respectively. The patent describes an example in which the message 520a is first received at the fourth processor 14 (column 8, lines 46-47). Upon receipt of this message, the processor examines an attribute field in the message and recognizes that another version of the same program exists. In response, the processor 14 sets a timer, to wait for the reception of the message 520b. When the processor 14 receives the message 520b it stores the message and waits for the timer to time out. Then, selection logic compares the results contained in the two messages 520a and 520b, and selects one of them in accordance with established criteria. An application program 54 is then executed in the processor 14 on the basis of the selected result.

From the foregoing, it can be seen that the Orimo patent discloses a system in which various processors execute respective application programs, and transmit the results of those programs as messages over a network. Other processors examine those messages, and select appropriate ones for use in the execution of their respective programs. In this arrangement, each processor contains its own memory for the storage of data (see Figure 3). There is no disclosure of a common memory in which data to be processed is stored and shared among the various processors. Rather, the data is transmitted from one processor to another by means of messages transmitted over the network.

The Office Action contends that it would be obvious to employ a shared memory in the system of the Orimo patent, in view of the teachings of the Tanenbaum reference. It is respectfully submitted, however, that the teachings of the Tanenbaum reference do not have any applicability to a system of the type disclosed in the Orimo patent. At pages 449-

450, the Tanenbaum reference discloses the sharing of objects between two or more processes. As an example, it describes the analysis of a digitized satellite image of the earth for use in weather forecasting, predicting crop harvest, and tracking pollution. The meteorological, agricultural and environmental programs that perform the analyses of the image are run as separate processes, which each map the photograph into its respective address space. By using this approach, all three processes can work on the same file at the same time.

The Tanenbaum reference does not pertain to a system in which multiple processes are performed on the same data in a prescribed order. Rather, in the example described in the Tanenbaum reference, each of the meteorological, agricultural and environmental programs run *independently* of one another. Thus, while they may all operate upon the same item of data, each one does so without regard to the results produced by the others. Consequently, since there is no coordination among the operations of the three programs, there is no need to store state information in the shared memory. Such information would not have any value, since none of the programs rely upon data produced by the other programs.

Since the Tanenbaum reference is directed to a system having a significantly different type of objective, and operation, from that disclosed in the Orimo patent, it would not be obvious to employ the teachings of that reference in the system of the Orimo patent. More importantly, there is no disclosure in the Tanenbaum reference that would teach one of ordinary skill in the art how to employ a shared memory in the system of the Orimo patent. That patent relies upon messages transmitted over a network to transfer data from

one processor to another. It is not directed to a system in which each of the processors performs independent operations on the same item of data, as in the Tanenbaum patent. There is no disclosure in either reference that would teach one how to use a shared memory to transmit messages from one processor to another in the system of the Orimo patent. Accordingly, it is respectfully submitted that it would not be obvious to combine the teachings of the Orimo patent and the Tanenbaum reference in the manner suggested in the Office Action.

Furthermore, it is respectfully submitted that the pending claims recite additional features of the invention that are neither disclosed nor suggested in the Orimo patent, whether considered by itself or in combination with the Tanenbaum reference. For example, claim 4 recites that the data processing system includes a first controller for controlling the plurality of processors to execute the series of processes, based on the state information. With reference to this claim, the Office Action generally refers to Figure 1 of the Orimo patent, as well as column 4, lines 4-9 and column 5, lines 27-39. However, these portions of the patent do not illustrate a controller that controls a *plurality* of processors to execute their respective processes based on state information. Rather, as recognized in the Office Action, each processor controls *itself*. There is no disclosure of a controller that controls a plurality of processors, particularly on the basis of state information.

Claim 5 further recites that the first controller rewrites the state information in response to the completion of each process by the plurality of processors. Since the Orimo patent does not disclose a first controller, as discussed above, it cannot be interpreted to

disclose this additional feature of the invention. Rather, each processor of the Orimo patent operates on its own, and sends out messages with the results of its operation.

Claim 6 recites a second controller for determining an attribute of data to be processed, wherein the second controller rewrites the state information in order to change the order of executing the series of processes if data is determined to have a prescribed attribute. While the Orimo patent mentions attributes, those attributes merely serve to identify whether two or more versions of a program exist. There is no disclosure in the patent suggesting that the attribute information is used by a controller in order to change the order of execution of processes on an item of data.

Claim 8 recites that the memory has one region to store state information corresponding to a single region where data to be processed is stored. This claim relates to the stored format illustrated in Figure 2, where each 8-bit region of data has an associated 3-bit state flag. In other words, claim 8 recites a one-to-one relationship between the state information and the data items.

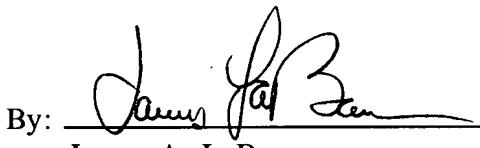
Claim 9 recites that the shared memory has one region to store state information corresponding to a plurality of regions where data to be processed is stored. This claim pertains to the format illustrated in Figure 8, where a single 3-bit state flag is associated with multiple 8-bit data regions.

Since the Orimo patent does not disclose a shared memory, as discussed above, it is respectfully submitted that it cannot be interpreted to suggest the particular formats recited in either of claims 8 or 9.

For the foregoing reasons, it is respectfully submitted that the subject matter of claims 1-10 is neither disclosed nor otherwise suggested by the Orimo patent, whether considered by itself or in combination with the Tanenbaum reference. For the same reasons, claims 11-20 are likewise submitted to be patentable over the cited references. Reconsideration and withdrawal of the rejection, and allowance of all pending claims is respectfully requested.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

By: 

James A. LaBarre
Registration No. 28,632

P.O. Box 1404
Alexandria, Virginia 22313-1404
(703) 836-6620

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Mark-up of Abstract

A data processing system has the following construction in order to reduce the memory capacity and the cost. [There are provided a] A plurality of processors [to execute to input image data] perform a series of processings on input image data in a prescribed order, including Log conversion, MTF correction, gamma correction and binarization [in a prescribed order and a memory to store]. A shared memory stores pixel data to be processed, and a state flag is used to represent the state of processing of the [pixel] data for each pixel in association with each other. Processings by the plurality of processors are executed asynchronously. [The plurality of processors share the memory.]

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Mark-up of Specification

Paragraph beginning at Page 2, line 29:

In order to solve this [program] problem, a circuit configuration in which image input device 2, processing portions 3 to 6 and image output device 7 are connected in an asynchronous manner, so as to be operated in response to independent clocks, may be considered. Fig. 19 is a block diagram for explaining a circuit configuration in which processing blocks are connected in an asynchronous manner. Referring to Fig. 19, processing blocks A, B and C can operate to perform processing in response to clock signals specific to them.

Paragraph beginning at Page 5, line 30:

Processing portion 9 performs Log conversion processing for each [of the] pixel [data] of the image data input by image input device 8. Processing portion 10 performs MTF correction to data after the Log conversion at processing portion 9. Processing portion 11 performs gamma correction to the data after the MTF correction at processing portion 10. Processing portion 12 binarizes the data after the gamma correction at processing portion 11. The four processings, the Log conversion, MTF correction, gamma correction and binarizing are the same as those previously described. The input processing by the image input device and the output processing by the image output device are the same as those performed by image input device 2 and image output device 7 described above and therefore the description is not repeated.

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Paragraph beginning at Page 6, line 16:

The data format of image data stored in memory 14 will be now described. Image data consists of a set of a plurality of pieces of pixel data. Referring to Fig. 2, pixel data is stored in a format formed of a 3-bit state flag region and a 8-bit data region. [The] A state flag [regions] region and a data [regions as many as the number of pieces] region for each piece of pixel data will be stored in memory 14.

Paragraph beginning at Page 6, line 28:

The state flag will be now described. The state flag represents [up to] which ones of the processing by processing portions 8 to 13 the pixel data has been through, in other words the flag represents which processing is to be performed next. Fig. 3 is a table for use in illustration of the state flag. The state flag is represented by a 3-digit binary number, in other words by 3 bits. If the state flag is "000", the flag represents that the pixel data stored in the data region is data input by image input device 8 and data which can be subjected to Log conversion by processing portion 9. If the state flag is "001", the flag represents that the pixel data stored in the data region has been subjected to Log conversion, and can be subjected to MTF correction at processing portion 10. Similarly if the state flag is "010", the data has been subjected to MTF correction and can be subjected to gamma correction. If the state flag is "011", the data has been subjected to gamma correction and can be binarized. If the state flag is "110", the data has been binarized and can [has] have its image output. If the state flag is "111", the data has its image output.

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Paragraph beginning at Page 9, line 24:

In this embodiment image data is stored in memory 14 in the format having the state flag region and data region for each pixel data piece (see Fig. 2), but one state flag may be provided for a plurality of pieces of pixel data, and a format having one state flag region and a plurality of data regions may be employed. Fig. 8 shows an example of such a format having one state flag region and a plurality of data regions. The format shown in Fig. 8 is effective for example if one state flag is provided for one line of pixel data pieces, or the image data is divided into 3×3 or 5×5 matrices and the pixel data included in each matrix is provided with one flag. If the format shown in Fig. 8 is used, processing portions 9 to 12 each read plural pieces of pixel data for each state of the [format] flag shown in Fig. 8 for executing processing.

Paragraph beginning at Page 10, line 15:

Referring to Fig. 9, a data processing apparatus according to a second embodiment of the invention includes a state control portion 20 in addition to the construction according to the first embodiment. State control portion 20 is connected to an image input device 8, processing portions 15 to 18, and an image output [device13] device 13, and controls these elements. Other than the processings by state control portion 20 and processing portions 15 to 18, the data processing apparatus according to the second embodiment is the same as the data processing apparatus according to the first embodiment, and the description is not repeated here.

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Paragraph beginning at Page 11, line 10:

It is then determined if the final pixel data, in other words, the data which has been read in the end by image input device 8 has the flag "110", and if the flag is "110" (step S14), the control proceeds to step S15. The control otherwise proceeds to step S11 and the process from steps S11 to S13 is repeated.

Paragraph beginning at Page 11, line 32:

Once the processing to the read image data has been completed, the processed data is written in memory 14 (step S23). The address to which the data is written at this time is the address received from state control portion 20 in step S20. Once the writing to memory 14 is completed, an end signal is transmitted to state control portion 20 (step S24).

Paragraph beginning at Page 12, line 16:

Region determining portion 30 determines whether or not pixel data input at image input device 8 is pixel data of a solid image before Log conversion by processing portion 15.

Paragraph beginning at Page 13, line 17:

Referring to Fig. 14, in the region determining processing, if the data is determined to be solid image data, the state flag is rewritten into ["110"] "100". The image data having the state flag rewritten into ["110"] "100" is then subjected to binarizing.

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Paragraph beginning at Page 15, line 11:

The state flag of the data processing apparatus according to the fourth embodiment will be now described. Referring to Fig. 17, if region determining portion 46 determines that pixel data is solid image data, the state flag is rewritten into ["110"] "101" and otherwise rewritten into "001".

Paragraph beginning at Page 15, line 15

In processing portion 41 to execute color conversion processing, pixel data having a state flag of "001" or ["100"] "101" is subjected to color conversion. As for pixel data having a state flag of "001", the state flag is rewritten into "010", and as for pixel data having a state flag of ["100"] "101", the state flag is rewritten into "110" after the completion of the color conversion.

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Mark-up of Claims 1, 3, 5, 6, 8-13, 15, 16, and 18-20

1. (Amended) A data processing system comprising:

a plurality of processors for executing a series of processings [to] on data to be processed, in a prescribed order; and

a memory for storing said data to be processed [and] in association with state information to represent the processing state of said data [in association with each other], wherein

processings executed by said plurality of processors are asynchronously executed and said plurality of processors share said memory.

3. (Amended) The data processing system according to claim 2, wherein

said plurality of processors each execute a processing [to] on said data to be processed, and then rewrite said state information corresponding to the processed data.

5. (Amended) The data processing system according to claim 4, wherein

said first controller rewrites said state information corresponding to processed data in response to the completion of each [of processings] processing by said plurality of processors.

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6. (Amended) The data processing system according to claim 1, further comprising a second controller for determining [the] an attribute of said data to be processed, wherein

said second controller rewrites said state information corresponding to said data to be processed in order to change the order of executing said series of processings if it is determined that said data to be processed has a prescribed attribute.

8. (Amended) The data processing system according to claim 1, wherein

said memory has one region to store said state information corresponding to [one] a single region [to store] where said data to be processed is stored.

9. (Amended) The data processing system according to claim 1, wherein

said memory has one region to store said state information corresponding to a plurality of regions [to store] where said data to be processed is stored.

11. (Amended) A data processing system, comprising:

a plurality of processing means for executing a series of processings [to] on data to be processed, in a prescribed order; and

memory means for storing said data to be processed [and] in association with state information to represent the processing state of said data [in association with each other], wherein

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processings executed by said plurality of processing means are executed asynchronously, and said plurality of processing means share said memory means.

13. (Amended) The data processing system according to claim 12, wherein said plurality of processing means each execute a processing [to] on said data to be processed and then rewrite said state information corresponding to the processed data.

15. (Amended) The data processing system according to claim 14, wherein said first control means rewrites said state information corresponding to processed data in response to the completion of each [of processings] processing by said plurality of processing means.

16. (Amended) The data processing system according to claim 11, further comprising a second control means for determining [the] an attribute of said data to be processed, wherein

if it is determined that said data to be processed has a prescribed attribute, said second control means rewrites said state information corresponding to said data to be processed in order to change the order of executing said series of processings.

18. (Amended) The data processing system according to claim 11 ,wherein

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said memory means has one region to store said state information corresponding to [one] a single region [to store] where said data to be processed is stored.

19. (Amended) The data processing system according to claim 11, wherein said memory means has one region to store said state information corresponding to a plurality of regions [to store] where said data to be processed is stored.